What is claimed is:

1. A clock generator comprising:

a receiving circuit to receive an external clock signal to produce an internal clock signal;

a data receiver to receive an external data signal to produce an internal data signal;

a first delay locked loop (DLL) to receive the internal clock signal to produce an output clock signal, wherein the output clock signal is 90 degrees out of phase with the internal clock signal; and

a second DLL selectively connected to the first DLL to receive the output clock signal to generate a capture clock signal, wherein the capture clock signal is 90 degrees out of phase with the internal data signal.

2. The clock generator of claim 1, wherein the external clock signal is edge aligned with the external data signal.

3. The clock generator of claim 1, wherein the receiving circuit includes a clock receiver and a data receiver model, wherein a delay of the data receiver model is the same as a delay of the data receiver.

4. The clock generator of claim 1, wherein the first DLL includes:

a first delay line to provide a quarter of clock cycle delay to the internal clock signal to generate the output clock signal;

a second delay line to provide a quarter of clock cycle delay to the output clock signal to generate a feedback signal;

a phase detector to compare an inverse of the internal clock signal and the feedback signal; and

a controller to provide control to the first and second delay lines.

5. The clock generator of claim 1, wherein the second DLL includes:

a forward path comprising:

a clock receiver;

a delay line to apply an amount of delay to the output clock signal to generate a delayed signal; and

a clock tree to receive the delayed signal to generate the capture signal; and

a feedback path to provide a feedback signal, the feedback path including a model circuit, wherein a delay of the model circuit includes a delay of the clock receiver.

6. The clock generator of claim 5, wherein the feedback signal of the second DLL and the output clock signal of the first DLL are synchronized.

7. A clock circuit comprising:

a receiving circuit to receive an external clock signal to produce an internal clock signal;

a data receiver to receive an external data signal to produce an internal data signal;

a first delay locked loop (DLL) to receive the internal clock signal to produce a slave output clock signal, wherein the slave output clock signal is one-fourth clock cycle delayed from the internal clock signal; and

a master DLL connected to the slave DLL, the master DLL comprising:

a forward path to receive the slave output clock signal to produce a capture clock signal; and

a feedback path to receive the capture clock signal to produce a feedback signal, wherein the capture clock signal is center aligned with the internal data signal when the feedback and slave output signals are synchronized.

8. The clock circuit of claim 7, wherein the external clock signal is edge aligned with the external data signal.

9. The clock generator of claim 7, wherein the receiving circuit includes a clock receiver and a data receiver model, wherein a delay of the data receiver model is the same as a delay of the data receiver.

10. The clock generator of claim 7, wherein the first DLL includes:

a first delay line to apply a quarter of clock cycle delay to the internal clock signal produce the slave output clock signal;

a second delay line to apply a quarter of clock cycle delay to the slave output clock signal to produce a slave feedback signal;

a phase detector to compare an inverse of the internal clock and slave feedback signals to provide shifting signals; and

a controller to control the first and second delay lines based on the shifting signals to keep the inverse of the internal clock and slave feedback signals synchronized.

11. The clock generator of claim 7, wherein the forward path includes:

a delay line to apply a delay to the output clock signal to generate a delayed signal; and

a clock tree to receive the delayed signal to generate a plurality of the capture clock signals.

12. The clock circuit of claim 7, wherein the forward path includes a clock receiver, the feedback path includes a model circuit, wherein a delay of the model circuit includes a delay of the clock receiver.

13. A clock circuit comprising:

a receiving circuit to receive an external clock signal to produce an internal clock signal;

a data receiver to receive an external data signal to produce an internal data signal;

a first delay locked loop (DLL) comprising:

a forward path to provide a slave output clock signal; and

a feedback path to provide a feedback signal, wherein the slave output clock signal is 90 degrees out of phase with the internal clock signal when the feedback signal and an inverse of the internal clock signal are synchronized; and

a master DLL connected to the slave DLL, the master DLL comprising:

a forward path to receive the slave output clock signal to produce a capture clock signal; and

a feedback path to receive the capture clock signal to produce a feedback signal, wherein the capture clock signal is center aligned with the internal data signal when the feedback and slave output signals are synchronized.

14. A clock generator comprising:

a receiving circuit to receive an external clock signal to produce an internal clock signal;

a data receiver to receive an external data signal to produce an internal data signal;

a slave delay locked loop (DLL) to receive the internal clock signal to produce a slave output clock signal, wherein the slave output clock signal is 90 degrees out of phase with the internal clock signal; and

a master connected to the slave DLL, the master DLL comprising:

a delay line to apply an amount of delay to the slave output clock signal to generate a delayed signal;

a clock tree circuit to receive the delayed signal to generate a plurality of capture clock signals;

a model circuit to receive one of the capture clock signals to generate a master feedback signal;

a phase detector to provide shifting signals based on a phase difference between the slave output clock and the master feedback signals; and

a control circuit to control the delay line to adjust the amount of delay applied to the slave output clock signal such that when the slave output clock and master feedback signals are synchronized the capture clock signal is center aligned with the internal data signal.

15. The clock generator of claim 14, wherein the external clock signal is edge aligned with the external data signal.

16. The clock generator of claim 14, wherein the receiving circuit includes a clock receiver, a model circuit includes a model delay, wherein the model delay includes a delay of the clock receiver.

17. The clock generator of claim 14, wherein the receiving circuit includes a clock receiver and a model of the data receiver.

18. The clock generator of claim 17, wherein the model circuit includes a model of the clock receiver.

19. A clock generator comprising:

a receiving circuit to receive an external clock signal to produce an internal clock signal, the receiving circuit including a clock receiver and a model of a data receiver;

a data receiver to receive an external data signal to produce an internal data signal;

a slave delay locked loop (DLL) comprising:

a forward path to provide a slave output clock signal; and

a feedback path to provide a feedback signal, wherein the slave output clock signal is 90 degrees out of phase with the internal clock signal when the feedback signal and an inverse of the internal clock signal are synchronized;

a master DLL connected to the slave DLL, the master DLL comprising:

a delay line to apply an amount of delay to the slave output clock signal to generate a delayed signal;

a clock tree circuit to receive the delayed signal to generate a plurality of capture clock signals;

a model circuit to receive one of the capture clock signals to generate a

master feedback signal, wherein a delay of the model circuit includes a delay of the clock receiver;

a phase detector to provide shifting signals based on a phase difference between the slave output clock and the master feedback signals; and

a control circuit to control the delay line to adjust the amount of delay applied to the slave output clock signal such that when the slave output clock and master feedback signals are synchronized the capture clock signal is center aligned with the internal data signal.

20. A clock generator comprising:

a clock receiver an external clock signal to produce an internal clock signal;

a first delay locked loop (DLL) to receive the internal clock signal to produce an output clock signal, wherein the output clock signal is 90 degrees out of phase with the internal clock signal;

a second DLL selectively connected to the first DLL to receive the output clock signal to generate a capture clock signal; and

a data path circuit to receive an internal data signal and the capture clock signal to generated an output data signal, wherein the output data signal is center aligned with the external clock signal.

21. The clock generator of claim 20, wherein the forward path includes:

a delay line to apply a delay to the output clock signal to generate a delayed signal; and

a clock tree to receive the delayed signal to generate a plurality of the capture clock signals.

22. The clock generator of claim 20, wherein the feedback path includes a model circuit, wherein a delay of the model circuit includes a delay of the clock receiver and a delay of the data path circuit.

23. The clock generator of claim 20, wherein the model circuit includes a model of the clock receiver and a model of the data path circuit.

24. A clock generator comprising:

a clock receiver to receive an external clock signal to produce an internal clock signal;

a delay line to apply an amount of delay to the internal clock signal to generate a delayed signal;

a clock tree circuit to receive the delayed signal to generate a plurality of capture clock signals;

a model circuit to receive one of the capture clock signal to generate a feedback signal, wherein a delay of the model circuit is equal to a delay of the clock receiver and a delay of the data path circuit;

a phase detector to provide shifting signals based on a phase difference between the internal clock and the feedback signals;

a control circuit to control the delay line to adjust the amount of delay applied to the internal clock signal; and

a data path circuit to receive an internal data signal and the capture clock signal to generated an output data signal, wherein the output data signal is center aligned with the external clock signal.

25. A memory system comprising:

a memory device including a plurality of memory cells; and

a memory controller connected to the memory device, the memory controller comprising:

a receiving circuit to receive an external clock signal to produce an internal clock signal;

a data receiver to receive an external data signal from the memory device to produce an internal data signal;

a first delay locked loop (DLL) to receive the internal clock signal to produce an output clock signal, wherein the output clock signal is 90 degrees out of phase with the internal clock signal; and

a second DLL selectively connected to the first DLL to receive the output clock signal to generate a capture clock signal, wherein the capture clock signal is 90 degrees out of phase with the internal data signal.

26. The memory system of claim 25, wherein the external data signal includes a data signal stored in one of the memory cells.

27. The memory system of claim 25, wherein the external data signal includes a data signal read from one of the memory cells during a read operation.

28. A memory system comprising:

a memory device including a plurality of memory cells; and

a memory controller connected to the memory device, the memory controller comprising:

a clock receiver an external clock signal to produce an internal clock signal;

a first delay locked loop (DLL) to receive the internal clock signal to produce an output clock signal, wherein the output clock signal is 90 degrees out of phase with the internal clock signal;

a second DLL selectively connected to the first DLL to receive the output clock signal to generate a capture clock signal; and

a data path circuit to receive an internal data signal and the capture clock signal to generated an output data signal, wherein the output data signal is center aligned with the external clock signal.

29. The memory system of claim 27, wherein the output data signal includes an address signal provided to the memory device during a memory write operation.

30. The memory system of claim 27, wherein the output data signal includes a control signal provided to the memory device during a memory write operation.

31. A system comprising:

a processor;

a memory device connected to the processor, the memory device including a plurality of memory cells to store data; and

a memory controller connected to the memory device, the memory controller comprising:

a receiving circuit to receive an external clock signal to produce an internal clock signal;

a data receiver to receive an external data signal from the memory device to produce an internal data signal;

a slave delay locked loop (DLL) to receive the internal clock signal to produce a slave output clock signal, wherein the slave output clock signal is 90 degrees out of phase with the internal clock signal; and

a master DLL selectively connected to the first DLL to receive the slave output clock signal to generate a capture clock signal, wherein the capture clock signal is 90 degrees out of phase with the internal data signal.

32. A system comprising:

a processor;

a memory device connected to the processor, the memory device including a plurality of memory cells to store data; and

a memory controller connected to the memory device, the memory controller comprising:

a clock receiver an external clock signal to produce an internal clock signal;

a first delay locked loop (DLL) to receive the internal clock signal to produce an output clock signal, wherein the output clock signal is 90 degrees out of phase with the internal clock signal;

a second DLL selectively connected to the first DLL to receive the output clock signal to generate a capture clock signal; and

a data path circuit to receive an internal data signal and the capture clock signal to generated an output data signal, wherein the output data signal is center aligned with the external clock signal.

33. A method of generating a capture clock signal, the method comprising:

receiving an external clock signal;

receiving an external data signal;

generating a output clock signal based on the internal clock signal, wherein the output clock signal is 90 degrees out of phase with the internal clock signal;

generating a capture clock signal based on the output clock signal; and

generating a feedback signal from the capture clock signal such that the capture clock signal is center aligned with the internal data signal when the feedback and output signals are synchronized.

34. The method of claim 33, wherein generating a capture clock signal include passing a delay signal generated from the internal clock signal to a clock tree circuit.

35. The method of claim 33, wherein receiving an external clock signal includes passing the external clock signal through a clock receiver.

36. The method of claim 35, wherein receiving an external data signal includes passing the external data signal through a data receiver.

37. The method of claim 36, wherein generating a feed back signal include passing the capture clock signal through a model circuit, wherein a delay of the model circuit includes a delay of the clock receiver.

38. A method of capturing a signal, the method comprising:

receiving an internal data signal;

generating an output clock signal from an internal clock signal, wherein the output clock signal is 90 degrees out of phase with the input clock signal;

generating a capture clock signal from the output clock signal; and

capturing the data signal such that the capture clock signal is center aligned with the internal data signal.

39. The method of claim 38 further includes:

passing an external clock signal through a receiving circuit having a clock delay;

passing an external data signal through a data receiver having a data delay;

generating a feedback signal from the capture clock signal by passing the capture clock signal through a model circuit, wherein a delay of the model circuit includes the clock delay; and

synchronizing the internal clock and the feedback signals.

40. A method of generating a signal, the method comprising:

receiving an external clock signal to generate an internal clock signal;

generating an output clock signal based on the internal clock signal, wherein the output clock signal is 90 degrees out of phase with the input clock signal;

generating a capture clock signal based on the output clock signal; and

capturing an internal data signal with the capture clock signal to produce an output data signal, wherein the output data signal is center aligned with the external clock signal.

41. The method of claim 60 further includes generating a feedback signal by delaying the capture clock signal.

42. The method of claim 41, wherein delaying the capture clock signal includes passing the capture clock signal through a modeled delay.

43. The method of claim 42 further includes:

passing the external clock signal through a clock receiver; and

passing the internal data through a data receiver, wherein a delay of the clock receiver and a delay of the data receiver are included in the model delay.